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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,367	NANJO ET AL.	
	Examin r	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *1-9 and 13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-12,27 and 28* is/are rejected.

7)☒ Claim(s) *25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is an official response to the amendment filed 22 August 2003. The amendment added claims 25-28. Currently, claims 1-28 are pending. Claims 1-9 and 13-24 have been withdrawn from further consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claims 10, 11, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 5,610,088 B1) in view of Kapoor (US 5,780,350 B1) and Wolf (Silicon Processing for the VLSI Era: Vol. 2 – Process Integration).*

Chang et al. disclose a method of manufacturing a semiconductor device (figs. 2A-2G and accompanying text). The method comprises the following steps substantially as claimed: preparing a semiconductor substrate 100 having first and second regions of a first conductivity type, p-type, defined in a principal surface area of the substrate (fig. 2A);[1] forming at least a first gate electrode 120 in a partial area of the first region (fig. 2A); implanting impurities of a second conductivity type, n-type,

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[1] See Appendix A.

opposite to the first conductivity type into a surface layer of the second region to form a first impurity diffusion region, n-well 110 (fig. 2A); forming first spacer film 134 on the side surface of the first gate electrode 120 (fig. 2C); by using the first gate electrode and the first spacer film as a mask, implanting impurities of the second conductivity type into a surface layer of the first region to form second impurity diffusion region, heavily doped source/drain 220 (fig. 2C); removing the first spacer film 134 (fig. 2D); and by using the first gate electrode as a mask, implanting impurities of the second conductivity type into a surface layer in the first region to form a third impurity diffusion region, LDD 222 (fig. 2D).

Chang et al. do not teach executing first, second, and third activation processes following the first, second, and third implanting steps, respectively; or executing each of the first to third activation processes at a temperature at least equal to 750°C.

Wolf discloses a method for forming an n-well in a CMOS integrated circuit (pages 428-431). The method comprises the steps of: implanting n-type impurities into a surface of a semiconductor substrate, and thereafter executing an activation process using a thermal treatment to form the n-well (page 430, fig. 6-35(a) and page 428, par. 5 – page 430, par. 1).[2]

Kapoor discloses a method for forming an integrated circuit (figs. 3-9 and accompanying text). The method comprises the steps of: forming first spacer film 30 on

[2] Inherently, the activation process is performed at a temperature of at least 750°C because a temperature of at least 750°C is required to activate and diffuse the implanted dopant impurity.

the side surface of a first gate electrode 12 (fig. 3); by using the first gate electrode and the first spacer film as a mask, implanting n-type impurities into a surface layer of a substrate, and thereafter executing an activation process using a thermal treatment to form heavily doped source/drain region 36/38 (fig. 4 and col. 4, lines 54-64);[3] removing the first spacer film 30 (fig. 7); and by using the first gate electrode as a mask, implanting n-type impurities into a surface layer in the substrate, and thereafter executing an activation process at a temperature of 950°C to form LDD 56/58 (fig. 8 and col. 5, lines 49-62). This activation process is sufficient to cause the gradient of an impurity concentration distribution in a p-n junction formed by the third impurity diffusion region 222 of Chang et al. to become steeper than the gradient of an impurity concentration distribution in a p-n junction formed by the first impurity diffusion region 110, and steeper than the gradient of an impurity concentration distribution in a p-n junction formed by the second impurity diffusion region 220.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to execute first, second, and third activation processes following the first, second, and third implanting steps, respectively, because the n-well 110, heavily doped source/drain 220, and LDD 222 are not formed until the dopant impurities are activated.

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[3] See footnote no. 1.

3. *Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Kapoor and Wolf as applied to claim 10 above, and further in view of Shibata (US 4,622,735 B1).*

As discussed above, Chang et al. teach using a first gate electrode as a mask, implanting impurities of the second conductivity type into a surface layer in the first region to form a third impurity diffusion region, LDD 222. Again, Kapoor teaches using a gate electrode as a mask, implanting n-type impurities into a surface layer in the substrate, and thereafter executing an activation process to form LDD 56/58. Neither Chang et al. , Wolf, or Kapoor teach, separately or combined, the limitation of using a laser thermal process for the third activation process.

Shibata discloses a method for forming an integrated circuit (e.g. figs. 1A-1G and accompanying text). The method comprises implanting impurities, and using a laser thermal process for the activation of source/drain regions (col. 3, lines 21-31).

One having ordinary skill in the art would have been motivated to modify the combination of Chang et al., wolf, and Kapoor, at the time the invention was made, by using a thermal process for the third activation process because laser annealing allows the substrate to be heated to a high temperature. Heating the substrate to a high temperature results in excellent crystallinity, as compared to rapid thermal processing. Laser annealing results in source/drain regions with lower resistivity.

4. *Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Kapoor, Wolf, and Shibata as applied to claim 12 above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

Neither Chang et al. , Wolf, Kapoor, or Shibata teach, either separately or combined, the limitation of using rapid thermal annealing for the first and second activation processes.

The Wolf et al. reference (Wolf Vol. 1) discloses the use of rapid thermal annealing to diffuse implanted impurities (page 307, line 32 – page 308, line 7).

One having ordinary skill in the art would have been motivated to modify the combination of Chang et al., Wolf (Vol. 2), Kapoor, and Shibata, at the time the invention was made, by using rapid thermal annealing for the first and second activation processes because, as Wolf (Vol. 1) teaches, rapid thermal annealing anneals implantations with minimal redistribution (page 307, lines 25-31).

Allowable Subject Matter

5. Claims 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Chang et al. does not anticipate, teach, or suggest that the step of implanting impurities of a second conductivity type into a surface layer of the second region to form a first impurity diffusion region forms a resistor. Instead, an n-well 110 is formed (fig. 2A). There is no teaching or suggestion within the prior art of record to modify Chang et al. such that the step of implanting

impurities of a second conductivity type into a surface layer of the second region forms a resistor. The prior art of record does not anticipate, teach, or suggest a method of manufacturing a semiconductor device comprising the process steps substantially as claimed, wherein impurities of a second conductivity type opposite to the first conductivity type are implanted into a surface layer of the second region to form a first impurity diffusion region, the first impurity region forming a resistor.

Response to Arguments

6. Applicant's arguments filed 22 August 2003 have been fully considered but they are not persuasive.

7. Applicant argues that "the first and third impurity diffusion regions are of the same conductivity type formed in respective surface layers of the second and first region of the first conductivity type, but are formed separately to realize a steep gradient of an impurity concentration distribution in the first region, and a gentle gradient of an impurity concentration in the second region."

As discussed previously in this Office action, Chang et al. discloses the steps of: implanting impurities of a second conductivity type, n-type, opposite to the first conductivity type into a surface layer of the second region to form a first impurity diffusion region, n-well 110 (fig. 2A); and by using the first gate electrode as a mask, implanting impurities of the second conductivity type into a surface layer in the first region to form a third impurity diffusion region, LDD 222 (fig. 2D). The first and third impurity diffusion regions are formed separately.

8. Applicant argues that none of the cited references teach or suggest the feature wherein the third impurity diffusion region can form a shallow extension (LDD) region for a short-channel high speed MOS transistor, while the first impurity diffusion region of gentle impurity concentration gradient can form a resistor of low leak current.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the feature upon which applicant relies is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TMT
30 October 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Appendix A

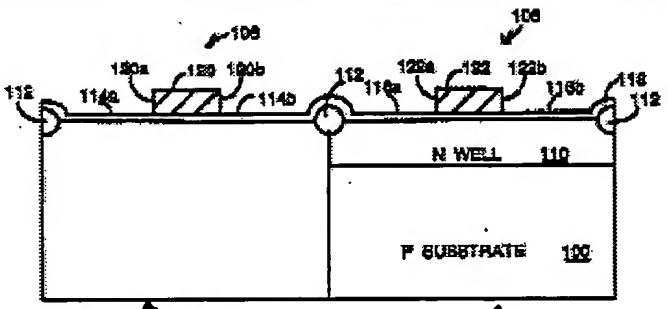

FIG. 2A

1st region

2nd region